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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/715,812 | 11/18/2003 | Jong-Hoon Oh | 2003P52888US | 5194 |

46798 7590 04/04/2005

MOSER, PATTERSON & SHERIDAN, LLP
GERO G. MCCLELLAN/INFINEON
3040 POST OAK BLVD.,
SUITE 1500
HOUSTON, TX 77056

| EXAMINER | |
|---|---|
| LE, THONG QUOC | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/715,812 | OH, JONG-HOON | |
| | Examiner | Art Unit | |
| | Thong Q. Le | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-1-23 are presented for examination.

### *Specification*

2. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Objections*

3. Claims 19 are objected to because of the following informalities: duplicated numbered claims. Appropriate correction is required.

There are two of claims is numbered 19.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimoto et al. (U.s. Patent No. 6,744,684).

Regarding claim 13, Arimoto et al. disclose a semiconductor memory device (Figure 6) , comprising:

a plurality of rows of memory cells (Figure 3, Column 9,54-60, Figure 6,41, Column 10, lines 51-53);

refresh circuitry (Figure 6, 50, Column 11, lines 36-46) configured to issue refresh requests (figure 6, FAY) for the rows of memory cells when the memory device is placed in a self-refresh mode (Column 4, lines 15-22, Column 11, lines 36-59);

row state circuitry (Figure 6, 58) configured to maintain a plurality of bits indicative of rows that are to be refreshed (Column 11, lines 4-25); and

refresh enable circuitry (Figure 6, 52) configured to limit the number of rows for which refresh requests are issued based on the bits of the row state circuitry (Column 11, lines 1-14).

Regarding claims 14-19, Arimoto et al. disclose wherein the refresh enable circuitry is configured to limit the number of rows for which refresh requests are issued by generating a signal (Figure 6, RADE) used to inhibit refresh requests (Column 11, lines 1-46), and wherein the signal is generated by accessing a bit corresponding to a row address generated by a refresh address counter (Figure 6, 54), and wherein the row state circuitry is configured to set bits to indicate rows of memory cells that have

been written to (Column 11, lines 1-14) ; and the refresh enable circuitry is configured to limit the number of rows for which refresh requests are issued to rows that have been written to, as indicated by the bits wherein each bit corresponds to a single row of memory cells (Column 11, lines 1-14), and wherein the row state circuitry is configured to maintain the set bits until the occurrence of a reset event (Column 13, lines 5-14).

Regarding claims 20-23, Arimotō et al. disclose a system Figure 1), comprising:

a memory device (MCR) having a plurality of rows of memory cells, wherein the memory device is configured to limit the number of rows that are refreshed, during a self-refresh mode, based on row data indicative of rows that are to be refreshed (Column 11, lines 1-59); and a memory controller (Figure 6, 40) configured to monitor write operations to the memory device, generate the row data based on the monitored write operations, and transfer the row data to the memory device prior to placing the memory device in the self- refresh mode (Column 10, lines 54-67), and wherein: the row data is stored in the memory device in an array of memory cells (Column 10, lines 48-67), and the memory controller is further configured to reset the array of memory cells prior to transferring the row data to the memory device (Figure 6, 40), and wherein the memory controller is configured to reset the array of memory cells by writing to a mode register of the memory device (Column 2, lines 16-49), and wherein the memory controller is configured to set a bit in the row data to indicate one or more cells in a corresponding row have been written (Column 11, lines 1-25).

Regarding claims 1-12, the apparatus discussed above would perform the claimed method 1-12.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER